KAYPRO 4 &

KAYPRO II THEORY OF OPERATION

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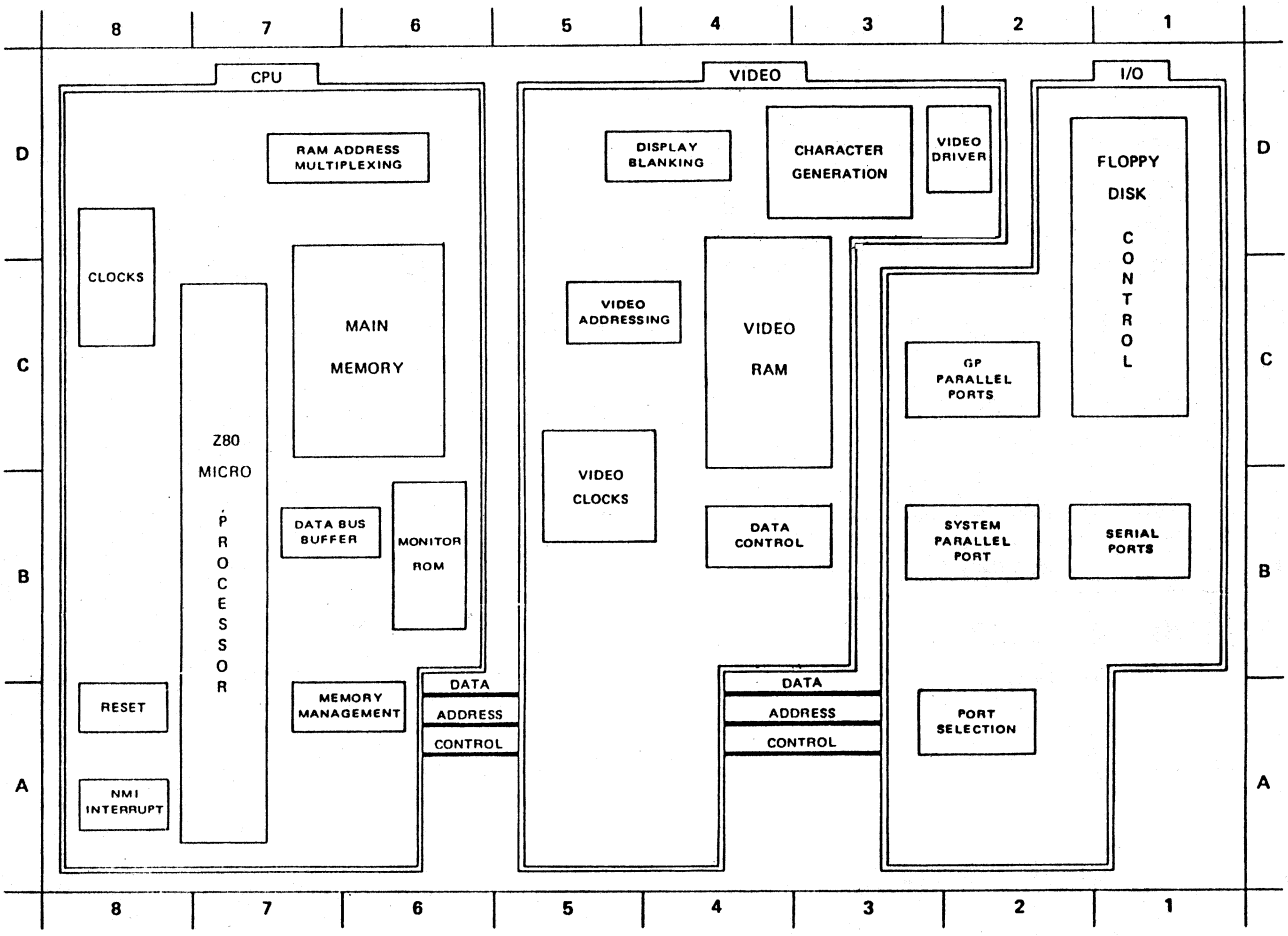


KAYPRO II BLOCK DIAGRAM

INTRODUCTION

This theory of operation is designed to help you use Micro Cornucopia's KayPro schematic and to help you better understand the system. We assume you have a basic understanding of digital circuits, but we also do our best to define all of the abbreviated symbols (alphabet soup) for those of you whose command of computerese is a bit weak.

The theory of operation begins with a diagram of the entire system. The blocks in this diagram are sized according to their relative importance in the section they appear. The diagram has the same basic layout as the schematic.

We've divided the KayPro into three sections—CPU (central processing unit), video, and I/O (input/output). Each section begins with its own block diagram.

The block diagrams show major subdivisions in the section as separate blocks. The perimeter of each block surrounds the approximate area that the circuit occupies on the schematic. The blocks are arranged so their grid coordinates correspond to the coordinates of the related circuitry.

The text that follows the block diagram describes the parts and signals responsible for the each circuit's function.

Where the circuits have been modified since the KayPro was introduced, both circuit forms are described.

Following the section description is a list of all integrated circuits used in that section.

A star following a signal label indicates that the signal is active low. For example, MREQ* is active low, but DRQ is active high. On the schematic, we use the usual form for active low (a line above the signal name).

The schematic was drawn to show all gates as positive logic. All active low inputs and outputs are designated with a bubble at the chip connection.

CIRCUIT OVERVIEW

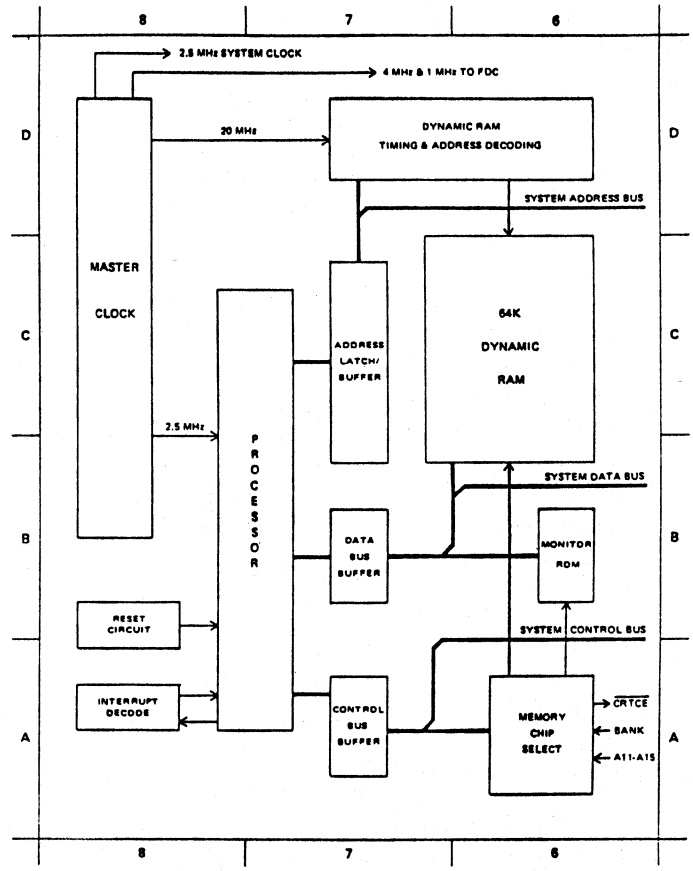
The KayPro design includes:

(1) CPU section with 64K of dynamic RAM and a system monitor in ROM. This section contains the data processing (CPU), fast access memory (RAM), the system clock (provides basic system timing), and the monitor ROM which contains the basic start-up and control routines.

This section oversees operation of the entire system, telling the video circuit what to display on the screen and commanding the I/O when to send or fetch data.

(2) Discrete video generator circuit. The CPU section sends characters along with information on where they should be displayed to this section. The video section then creates the video signal which locates those characters in their proper places on the video screen.

(3) I/O section. This portion of the system handles communications with the outside world. These communications include: the keyboard input, output/input of data to and from the floppy disk, parallel printer output, and input/output via the serial port.



CPU SECTION BLOCK DIAGRAM

CPU SECTION

The central processing unit of the KayPro II is a 2.5 MHz Z80 using 64K of RAM for main memory. User programs and CP/M reside in this 64K of RAM (called bank 0). The monitor (contained in the EPROM U47) and video RAM lie in a separate bank of memory called bank 1. Only the lower 16K of main memory (bank 0) is switched out when bank 1 is accessed.

All input/output operations are interrupt driven.

MASTER CLOCK—B8,C8,D8—

The master clock is responsible for providing the 2.5 MHz system clock, the 1 MHz floppy disk controller clock, and the 4 MHz double density timing clock. All of these frequencies are derived from a single oscillator running at 20 MHz. Video frequencies are produced by a separate 13.9776 MHz oscillator.

Master Oscillator—B8—

The master oscillator frequency is generated by a 20 MHz crystal, Y2. Inverter U67 drives the crystal.

C7, C8, and C9 help shape the waveform. A second inverter isolates the oscillator and turns the sine wave output into a square wave.

2.5 MHz Clock—C8—

20 MHz from the master oscillator goes to the A input (pin 10) of U86 (a flip-flop). The 10 MHz output of this flip-flop (QA pin 9) becomes the input for three series connected flip-flops.

Each flip-flop divides the frequency by two. So, 5 MHz is available at QB pin 5, 2.5 MHz is available at QC pin 4 (used as the system clock), and QD pin 8 outputs 1.25 MHz.

2.5 MHz Waveshaping—B8—

Early models of the KayPro II used Q1 and C6 to shorten signal rise time, but this has been omitted on later models.

FLOPPY CONTROLLER CLOCK—C8,D8—

4 MHz is generated by dividing the 20 MHz from the master oscillator by 5. Half of the dual decade counter, U87, accomplishes this division. The resulting square wave is not symmetrical and has a 40/60 duty cycle (high/low).

The first units shipped derived the 1 MHz controller clock differently. This was done by using the A flip-flop in U87 to divide the original 20 MHz by 2 and then using the other counter in the package to divide the resulting 10 MHz by 10.

Now the 1 MHz is derived as shown on the schematic. They feed 4 MHz to flip-flop A in U87, creating 2 MHz. The 2 MHz signal is then fed to flip-flop A in the other half of U87, which again divides the frequency by two. This gives you a 1 MHz signal that is synchronized with the 4 MHz.

RESET PULSE GENERATION—B8—

The power-on reset is a simple RC circuit. The way the circuit is designed, there is no way to guarantee that the contents of the system memory will be unchanged when the system is reset.

C20 must charge through the 10K resistor R32. Thus, the reset (RST*) signal will not go high until the power supply has had time to stabilize.

RST* is ORed with M1 to provide the I/O chips with an M1 reset (M1R*).

INTERRUPT DECODE—A8—

The floppy disk controller controls the non-maskable interrupt line (NMI*). DRQ and IRQ outputs from the 1793 are ORed by U61. The output from this gate is inverted by U73 and negative ANDed with the HALT* output from the processor. Its output is connected to the Z80's NMI* input.

The I/O chips interrupt the processor via INT*(U63 pin 16), the maskable interrupt line.

RAM TIMING AND ADDRESS DECODING—D6—

The main memory is made up of eight 64K by 1 dynamic RAMs (random access memories).

These 4164 (or equivalent) RAM chips receive their 16-bit addresses in two chunks, eight bits at a time.

This is accomplished by multiplexing the 16 bit address bus into 8 bits. The signal responsible for timing this multiplex is the MUX signal. There are two other signals that are necessary for timing the addressing. CAS (column address strobe) and RAS (row address strobe) tell the RAM when the addresses are valid.

Timing—D7—

CAS and MUX signals are generated by shift register U66. The register is clocked by the 20 MHz clock. MREQ* or RFSH* will clear the shift register. MREQ*does this to synchronize the generation of CAS and MUX to the pending memory access. RFSH* does this to prevent generation of CAS and MUX during a memory refresh.

The CAS signal is buffered through two inverters from U48. The resulting CAS* is fed to all the dynamic RAM chips.

The MUX signal goes to the SELECT inputs of the two-to-one multiplexers U33 and U34. A low on MUX selects the 'A' inputs and a high selects the 'B' inputs.

MEMORY CHIP SELECT—A6—

RAS Generation—A6—

RAS* (row address select) is developed by decoding A14 and A15 with BANK and RFSH* and gating it with MREQ*.

Bank Select Decode—A6—

The monitor ROM and the video memory are selected by the 3 to 8 line decoder, U60. Address lines 11-13 are the inputs for U60.

This decoder requires three different conditions. Bank 1 must be selected, A14 and A15 must both be low, and MREQ* must be active. Under these conditions, the monitor ROM occupies addresses 0000H-07FFH and the video RAM is located from 3000H-3BFFH.

MONITOR ROM—B6—

The monitor ROM is a 2716 (2K x 8) EPROM. It contains all the I/O routines, including disk operations.

ADDRESS BUS BUFFER—C7—

The lower 8 address lines are buffered through U49 which is always enabled. Only the 1793 floppy disk controller receives any unbuffered address signals.

The upper 8 address lines are latched by U59. This latch is needed because the Z80 processor does not keep the data stable on the address lines throughout the MREQ cycle. The MREQ* line controls the latch.

DATA BUS BUFFER—B7—

The data bus is buffered through two 4 bit tranceivers U64 and U65. In order for data to be directed to the processor, both MREQ* and RD* must be low. This prevents contention on the unbuffered I/O and the RAM.

CONTROL BUS BUFFER—A7—

Five of the buffers in U62 are used to buffer system control lines. These buffers are always enabled.

U#	Device	Location	Description
Y2	CRYSTAL	B8	20 MHz crystal
U20-27	MCM6665	D6	64K x 1 Dynamic RAM
U33	74LS157	D6	8 to 4 line decoder
U34	74LS157	D7	8 to 4 line decoder
U35	8216	C6	4 bit tranceiver
U38	8216	B6	4 bit tranceiver
U36	74LS20	A6	Dual 4 input positive NAND
U37	74LS02	A6	Quad 2 input positive NOR
U39	74LS00	A6	Quad 2 input positive NAND
U47	2716	B6	2K x 8 EPROM containing monitor
U48	74LS04	A6,D7	Hex inverters
U49	74LS241	B7	Octal buffers/line drivers
U56	74LS02	A6,D7	Quad 2 input positive NOR
U59	74LS373	C7	Octal D-latches/flip flops
U60	74LS138	A6	3 to 8 line decoder
U61	74LS32	A8,A6	Quad 2 input positive OR
U62	74LS241	A7	Octal buffers/line drivers
U63	3880	A7-C7	Z80 microprocessor
U64	74LS243	B7	Quad bus tranceivers
U65	74LS243	B7	Quad bus tranceivers
U66	74164	D7	8 bit parallel out shift register
U67	74HC04	B8	Hex inverters
U73	74LS04	A8	Hex inverters
U80	74LS08	A7,A5	Quad 2 input positive AND
U86	74LS293	C8	Decade counter
U87	74LS390	C8-D8	Dual decade counter

POWER CONNECTIONS

Power supply connections are not shown on the schematic. For the most part, the chips only need +5V and ground. When looking at an integrated circuit with pin −1 at the top, the +5V will be at the pin in the upper right corner (the highest numbered pin) on and ground will be at the lower left corner (half the highest numbered pin). So, on a 14 pin package, pin 14 is tied to +5V and pin 7 is grounded.

U68, (contains the RS-232 line drivers), requires +/−12 volts in order to provide RS-232 level outputs. +12V is supplied to the chip at pin 14 and −12V at pin 1. Five volts is not supplied to this chip.

Power is brought to the KayPro circuit board by connector J5. The connector pins are used as follows.

PIN	USE
1	no connection
2	-12 volts
3	+12 volts
4	ground
5	key
6	+5 volts

VIDEO SECTION

The video section on the KayPro delivers separate video and sync to the CRT circuit board. It employs software scrolling rather than an external scroll register. The routines responsible for the CRT display reside in the monitor ROM.

All clocks are derived from a master oscillator running at 13.9776 MHz. This frequency is used to develop the dot count. A character count is developed by dividing the master oscillator frequency by 7. The character counter is then divided by 128 to form the scan count. The scan counter is divided by 10 to drive the line counter which is divided by 26 to provide the frame clock.

The video sync signals are timed by decoding these counters. The horizontal sync is timed by decoding the eightieth count of the character clock. The vertical sync is timed by decoding line count twenty four.

All of the signals used by the CRT circuit board are available at solder pads E1-E6.

VIDEO OSCILLATOR—A5—

This oscillator (or clock) is the same design as the master oscillator in the CPU section but uses a 13.9776 MHz crystal as its frequency source. The clock is used to generate all video frequencies. The 2.5 MHz system clock is not found anywhere in the video section. Because of the clock differences between these two sections, the MREQ*, RD*, and WR* are used to synchronize data transfers.

DOT CLOCK GENERATION—A5—

The 13.9776 MHz from the video oscillator clocks a 4-bit binary counter, U1. This counter can count from 0 to 15, but it is pre-loaded with a 9 at the 15 count to accomplish a divide-by-7 function. This is done by a hard-wired binary 9 on the counter's inputs.

This 9 is parallel loaded into the counter when LD* (pin 9) is active. LD* is pulled active by the inverted ripple carry (RC) output from the same counter. The same signal is also used as the DCTC (device control timing clock) for other devices in the video section. The DCTC is a 1.9968 MHz clock. The binary count from U1 is used by the demultiplexer, U41, to clock out the dot information provided by the character ROM as a serial video signal.

CPU ACCESS DETECTOR—A5—

This circuit provides a display blanking request whenever the CPU is accessing video RAM. The D flip-flops in U12 assure that the blanking is synchronized to the DCTC.

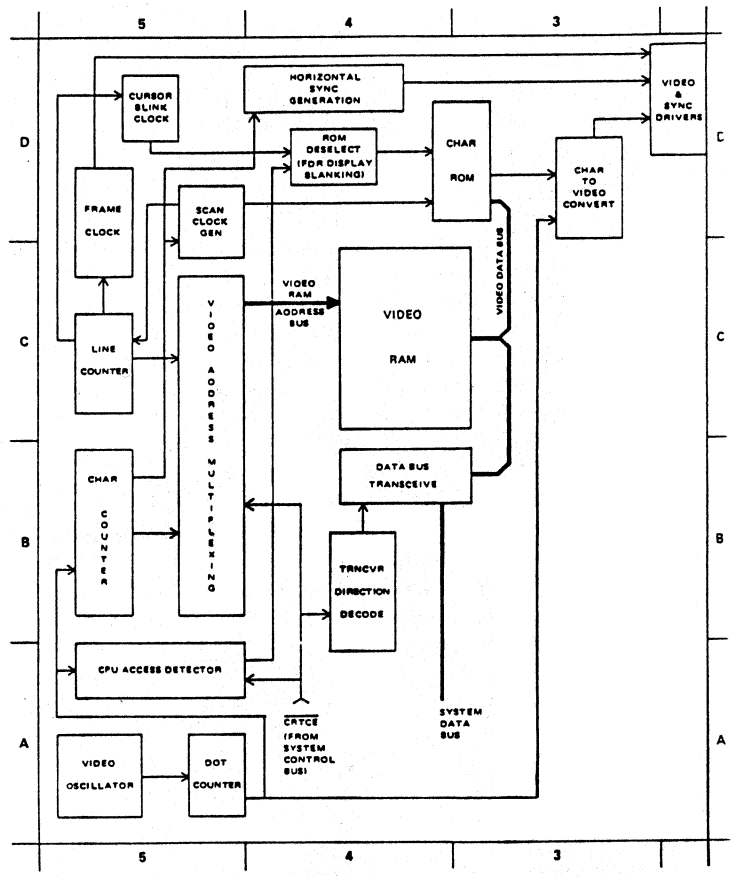
The output signal of this circuit is DC1. It is decoded along with other conditions by the character ROM deselection circuit.

CHARACTER COUNTER—B5—

DCTC is used to clock the character counter U6. Both of the binary counters in this chip are used to count to 128. The outputs feed the video RAM address multiplexers to provide character addresses. In addition, character clocks CC4, CC5, and CC6 are decoded to generate horizontal blanking.

SCAN COUNTER—D5—

Character clock CC6, which is DCTC divided by 128, is used to clock the scan counter. The scan count provides the character ROM with its 3 least significant address bits. These bits point at the horizontal line of dots in the character matrix that is to be displayed for a given scan line. SC3 is used to time blanking during the 9th and 10th horizontal dot lines of each character.



VIDEO SECTION BLOCK DIAGRAM

LINE COUNTER—C5—

The line counter is clocked by SC3 after SC3 has been divided by 2 by U14. The line counter provides the address multiplexers with the binary count needed to complete the video RAM address bus. The line clock LC4 is used to clock a shift register for use as the cursor blinking clock.

FRAME CLOCK—D5—

The line count is decoded to provide frame timing. This is used for vertical retrace blanking and vertical sync. The frame clock also resets the line counter after 24 lines.

VIDEO ADDRESS MULTIPLEXING—B5,C5—

U17, U18, and U19 create the video address bus for the video RAM. When CRTCE* is inactive, the addresses are derived from the character and line counters. When CRTCE* is active, the addresses are gated to the video RAM from the system address bus. U16 maps the addresses in the video memory array.

VIDEO RAM—C4—

2114 (1K x 4) static RAM chips are used for the video memory. Read and write signals are decoded from system control signals—RD*, WR*, and MREQ*. The information stored in the video RAM is ASCII data, which selects (by addressing the character ROM) the dot pattern for the character it represents. Bit 7 (the high bit) is not used in ASCII code; so it is available as a character attribute bit. When bit 7 is set the character blinks.

DATA BUS TRANCEIVERS—B4—

The system data bus is buffered through 4-bit tranceivers U44 and U45. The direction of data transfer is decoded by U58. The decoder is enabled by an active level on MREQ and CRTCE. When U58 is enabled, data may be read from or written to the video RAM by the CPU. If MREQ*, RD*, and WR* are all inactive, feedback from output 7 of U58 will disable the chip.

HORIZONTAL SYNC—D4—

Horizontal sync is timed by the decoding of the 80th character count by gates in U9 and U10. This timing pulse is fed into D flip-flop U32. When this flip-flop is clocked by dot clock DCB, it provides a horizontal sync pulse at its Q output. The Q* output of the same flip-flop is used to present a logic 0 at A10 of the character ROM (thus selecting the lower half of the character ROM). Since the lower half of the ROM is empty, this procedure blanks the display during horizontal retrace.

ROM DESELECT—D4—

All other display blanking is accomplished by disabling the character ROM. The gates in this block blank the display in response to three different conditions. U9 will blank the display for one character position if bit 7 is set (for that character) and there is a logic 1 on U9's other input. Since the signal to that input is connected to the cursor blinking clock, that character will blink.

The output of U9 is ORed by U10 with the output of the CPU access detector. The output of U10 is ORed with scan clock SC3, which blanks the display during the 9th and 10th horizontal scans of each line. This provides a space of two horizontal scans between the descenders of one line of characters and the highest points in the following line.

CHARACTER ROM—D3—

A 2716 (2K x 8) EPROM is used to store the dot information for every character displayed. Each character is set in an array of dots, 8 rows and 8 columns. Only 5 of the the columns are used for each character.

Eight bytes are used for each character, one for each row. Seven of the rows are used for the character body and the bottom row is used for descenders. The 0 bits are displayed as lighted dots.

The ASCII data in the video RAM points to the character and the scan clock adds the low order three bits to select which of the eight rows (0-7) of that character will be displayed.

Since only 5 columns are used, D5-D7 have no connections from the ROM.

CHARACTER TO VIDEO CONVERSION—D3—

As each row of dots is addressed, the hex D flip-flop U42, samples the byte as it is clocked in by DCTC. U41 then multiplexes the parallel dot pattern out to the video driver one dot at a time. While it is doing this, U42 is getting the dot pattern for the next character.

U#	Device	Location	Description
Y1	CRYSTAL	A5	13.9776 MHz crystal
U1	74LS161	A5	Parallel loading binary counter
U2	74HC04	A5	Hex inverters
U3	74LS290	D5	Decade counter
U4	74LS10	A4,C5	Triple three input positive NAND
U6	74LS393	B5	Dual 4 bit binary counters
U9	74LS08	C5,D2,D4	Quad 2 input positive AND
U10	74LS32	D4	Quad 2 input positive OR
U11	74LS393	C5,D5	Dual 4 bit binary counters
U12	74LS74	A5	Dual D-type flip-flops
U14	74LS74	C5,D5	Dual D-type flip-flops
U15	74LS00	C4,D2	Quad 2 input positive NAND
U16	74LS157	C5	2 to 1 line multiplexer
U17	74LS157	B5	2 to 1 line multiplexer
U18	74LS157	C5	2 to 1 line multiplexer
U19	74LS157	B5	2 to 1 line multiplexer
U28	2114	C5	1K x 4 static RAM
U29	2114	C5	1K x 4 static RAM
U30	2114	C5	1K x 4 static RAM
U31	2114	C5	1K x 4 static RAM
U32	74LS74	D4	Dual D-type flip-flops
U41	74LS151	D3	1 of 8 data multiplexer
U42	74LS174	D3	Hex D-type flip-flops
U43	2716	D4	2K x 8 EPROM containing character set
U44	74LS243	B4	Quad bus transceivers
U45	74LS243	B4	Quad bus tranceivers
U56	74LS02	B4	Quad 2 input positive NOR
U58	74LS138	B4	3 to 8 line decoder

I/O SECTION

The KayPro II uses Z80 programmable I/O chips for its ports. There are two parallel I/O chips (PIO) and one serial I/O chip (SIO). Each of these chips contains two individually addressable ports.

Both serial ports are used by the KayPro. One is the keyboard port and the other is an RS-232 port. The RS-232 port is connected to the DB-25 connector J4, and is considered to be TTY by the monitor.

One of the parallel ports is used by the system for control and selection purposes. Another is dedicated to the Centronics connector J2. The two parallel ports remaining are not used but their data connections are available at labeled solder pads.

The floppy disk controller uses 4 ports for communicating with the processor. These ports do not go through an I/O chip but are managed by the controller chip itself.

The following table describes the port assignments for all of the ports on the KayPro II.

Z80 I/O PORTS

PORT	TYPE	CNTL.	DATA	USE
A	serial	06H	04H	RS-232 (J4)
B	serial	07H	05H	Keyboard (J3)
gp/A	parallel	09H	08H	Centronics (J2)
gp/B	parallel	0BH	0AH	Not used (E7-E14)
sys/A	parallel	1DH	1CH	System bit port
				bit 0-disk drive A select
				bit 1-disk drive B select
				bit 2-not used
				bit 3-centronics ready flag
				bit 4-centronics data strobe
				bit 5-double density enable
				bit 6-disk drive motors
				bit 7-bank select
sys/B	parallel	1FH	1EH	8 bits unused (E29-E34)

DISK DRIVE CONTROLLER PORTS

ADDR.	IN	OUT
10H	status	command
11H	track	track
12H	sector	sector
13H	data	data

INTERRUPTS

The I/O ports in the KayPro are assigned priority by hardware design. The floppy disk controller has the highest priority so it controls processor's NMI input. The other I/O ports are daisy-chained together using the Z80 I/O IEO (interrupt enable out) and IEI (interrupt enable in) pins.

The highest priority chip has its IEI tied to 5 volts. The IEO from this chip goes to the IEI of the next highest priority chip. This continues for all the chips in the priority chain with the IEO of the last chip left unconnected. This way all the I/O chips use the INT* input to the processor with the interrupt priority resolution taken care of by the I/O devices themselves. The priority chain is as follows:

1. Floppy disk controller ports
2. Serial I/O ports
3. System parallel I/O (bitport)
4. General purpose parallel I/O (centronics)

I/O SELECT/DECODE—A3—

Each chip in the I/O (input/output) section, the 2 PIOs (parallel input/output), the SIO (serial input/output), and the FDC (floppy disk controller), decodes two address lines, A0 and A1. These two address lines tell each I/O chip which control or data register the processor wants to read from, or write to.

U57, a 3 to 8 decoder selects which chip is enabled. Address line A7 enables U57, so all port addresses lie between 00H and 7FH.

All I/O data is transferred over the unbuffered data bus. This sets the priority on I/O higher than for memory accesses. So the FDC can assert a non-maskable interrupt and gain quick access to the data bus in the earliest possible M1 cycle.

The use for the decoder's outputs is shown below.

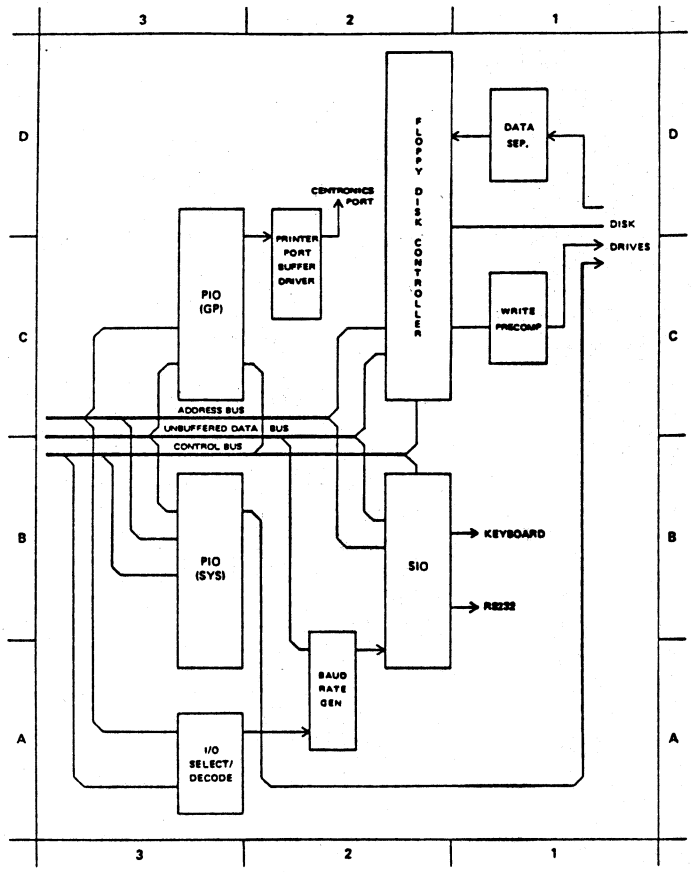
OUTPUT #	USE
0	Set baud A strobe
1	SIO chip enable
2	GP PIO chip enable
3	Set baud B strobe
4	FDC chip select
5	not used
6	not used
7	SYS PIO chip enable

BAUD RATE GENERATION—A2—

U78 is a programmable baud rate generator. All that it requires to provide software selectable baud rates for the SIO is a 5.0688 MHz crystal and access to the data bus. Only the lower nibble (4 bits) of the data bus is used, and these 4 bits set the baud rate for either port A or port B.

The address bus is decoded by U57 to provide the baud rate set strobe. When U78 sees a strobe on one of its STBX inputs, it examines D0-D3 and generates the selected frequency at the FX output. The baud rates are listed below.

BAUD	D0-D3	BAUD	D0-D3
50	00H	1800	08H
75	01H	2000	09H
110	02H	2400	0AH
134	03H	3600	0BH
150	04H	4800	0CH
300	05H	7200	0DH
600	06H	9600	0EH
1200	07H	19200	0FH



I/O SECTION BLOCK DIAGRAM

SERIAL I/O—B2—

The Z80 SIO, U70, has the highest interrupt priority of the I/O chips. The baud rate clock is provided by U78. The remaining serial communication operations are performed by this chip.

As an introduction to the SIO, the following list provides the function of some of the SIO pins.

B/A*	Selects between channel A and channel B
C/D*	Selects port use as control (C) or data (D)
CE*	Enables the internal data bus tranceivers
M1* and IORQ*	Interpreted by the SIO as an interrupt acknowledge
RST*	Disables RCVR and XMTR functions and clears all control registers
TxCA and TxCB	Transmitter clocks
RxCA and RxCB	Receiver clocks

In the KayPro the transmitter and receiver clocks are tied together so that the baud rate must be the same in both directions.

Channel B is dedicated to the keyboard. The keyboard for the KayPro outputs serial data at 300 baud. Only two of the SIO's pins are used for the keyboard, transmit data and receive data.

The transmit data line is used only for the keyboard bell. The system monitor sets the baud for channel B to 300 baud on initialization. All handshaking lines are ignored.

Channel A is used for an RS-232 port. This port is referred to by software as 'TTY'. This port is initially setup to handle 8 bits/character, 1 stop bit, no parity. The configuration program that comes with the KayPro only sets the baud rate. It doesn't let you set the number of bits/character, the number of stop bits, or parity.

Channel A uses nearly all of the RS-232 handshake lines. Following is a list of the DB-25 (J4) pin usage.

DB-25 pin	Mnemonic	Description
1		Frame ground
2	TxD	Transmit data
3	RxD	Receive data
4	RTS	Request to send
5	CTS	Clear to send
6	DSR	Data set ready
7		Signal ground
8	DCD	Data carrier detect
20	DTR	Data terminal ready

On the KayPro, frame and signal ground are tied together and to the ground bus. Pin 6 (DSR) is tied to 5 volts so it is high as long as the system is powered up. The other pins connect through line drivers to the SIO chip. U68 contains line drivers which output +12V and −12V RS-232 line levels for the RTS, DTR, and TxD lines. U69 contains RS-232 line receivers. It changes RS-232 signal levels to TTL signals for the SIO.

Software control of the SIO

The SIO is actually a more complex chip than the Z80. Programming it is not a trivial project, and I recommend that you find someone local who has done it a few times (preferably successfully) to help you get started. You'll save yourself a lot of time and frustration this way.

There are manuals on the SIO put out by the chip's manufacturers. Zilog's manual is complete, but it is no more readable than any of the others.

Basically, you need to send a string of bytes to the SIO control port (also called the status port) for side A. (Remember that side B of the SIO is dedicated to the keyboard so don't mess with that unless you don't plan to use your keyboard.)

SIO port A control is called port 06 in the KayPro. If you want to output new control information to that port, you would do something like:

```
LD      A,18H   ; (18H will reset the SIO)
OUT     06,A    ; (send the 18H to the SIO's register 0)
LD      A,01H   ; (01H will tell the SIO you want register 1)
OUT     06,A    ; (output the 01H to the SIO control port)
LD      A,00H   ; (00H in register 1 puts SIO in no-interrupt mode)
OUT     06,A    ; (send the 00H to register 1)
LD      A,04H   ; (04H will tell the SIO you want register 4)
OUT     06,A    ; (output the 04H to the SIO control port)
.
.
. (see below for complete example)
```

If you want to reconfigure the SIO, you first need to write to the control register which steers the following byte to the correct destination. This is control register WR0. When you output a byte of data to KayPro port 06, the data goes directly to the SIO's control register 0.

When you output a byte to control register 0, you can either use that byte as a direct command for the SIO, or you can use the byte to select another register (1-7).

You can use bits D0-D2 to indicate the target register for the next byte or you can use bits D3-D5 to specify a direct command to control register 0.

Register 0 command codes.

D3	D4	D5	COMMAND
0	0	0	select register with D0-D2
0	0	1	transmit abort (for SDLC mode)
0	1	0	reset status interrupts
0	1	1	reset one channel (the selected channel)
1	0	0	enable interrupt on next char. received
1	0	1	reset transmitter interrupt pending
1	1	0	reset error latches (18H in line 1 above)
1	1	1	return from interrupt (channel A only)

For most purposes, only 000 is used. Bits D6-D7 reset the CRC checkers and generators and are usually left at 00 also. The following table illustrates the pointer to each control register and its use.

WR1	interrupt mode select
WR2	interrupt vector
WR3	receiver parameters
WR4	parity/clock multiplier/stop bits
WR5	transmit parameters
WR6	for synchronous use
WR7	for synchronous use

Common Configurations for KayPro communications

REGISTER	BITS		FUNCTION
WR3	D7	D6	Receiver Bits/Character
	0	0	5 bits/char
	1	0	6 bits/char
	0	1	7 bits/char
	1	1	8 bits/char
		D0	Receive Enable (when set to 1)
		D5	Auto enable on CTS (when set to 1)
WR4	D3	D2	Stop Bits
	0	0	none (synchronous)
	0	1	one stop bit (most common)
	1	0	one and a half stop bits (least common)
	1	1	two stop bits
	D1	D0	Parity
	0	0	no parity
	0	1	odd parity
	1	1	even parity
		D6	16X clock (should be always set to 1)
WR5		D7	Assert DTR (when set to 1)
	D6	D5	Transmit Bits/character
	0	0	5 bits/char
	1	0	6 bits/char
	0	1	7 bits/char
	1	1	8 bits/char
		D3	Transmit Enable (when set to 1)

The following examples describe the commands required to set the SIO for some common operating modes.

7 BITS/CHARACTER, ODD PARITY, ONE STOP BIT

BIT(S)	SIGNIFICANCE	
D7-D6	clock multiplier	40H
D5-D4	synchronous mode	00H
D3-D2	1 stop bit	04H
D1	odd parity	00H
D0	enable parity	01H
Output to register 04H		**45H**
D7-D6	RCV 7 bits per character	40H
D5	if 1, DCD and CTS enable RCV and XMIT	00H
D4-D1	used for synchronous mode	00H
D0	RCV enable	01H
Output to register 03H		**41H**
D7	assert DTR	80H
D6-D5	XMIT 7 bits per char	20H
D4	send break	00H
D3	XMIT enable	08H
D2	used for synch. mode	00H
D1	controls RTS*in synch. mode	00H
D0	enable XMIT CRC	00H
Output to register 05H		**A8H**

So, let's look at a complete initialization of the SIO (a completed version of the above example).

```
LD      A,18H    ; (18H will reset the SIO)
OUT     06,A     ; (send the 18H to the SIO's register 0)
LD      A,01H    ; (01H will tell the SIO you want register 1)
OUT     06,A     ; (output the 01H to the SIO control port)
LD      A,00H    ; (00H in register 1 puts SIO in no-interrupt mode)
OUT     06,A     ; (send the 00H to register 1)
LD      A,04H    ; (04H will tell the SIO you want register 4)
OUT     06,A     ; (output the 04H to the SIO control port)
LD      A,45H    ; (45H in register 4 means 16X clock, 1 stop bit, odd
                   parity)
OUT     06,A     ; (send the 00H to register 1)
LD      A,03H    ; (03H will tell the SIO you want register 3)
OUT     06,A     ; (output the 03H to the SIO control port)
LD      A,41H    ; (41H in register 3 means 7 bits/RCV character,
                 ; non-synchronous, receiver enabled)
OUT     06,A     ; (send the 41H to register 3)
LD      A,05H    ; (05H will tell the SIO you want register 5)
OUT     06,A     ; (output the 05H to the SIO control port)
LD      A,A8H    ; (A8H in register 5 means DTR asserted,
                   7 bits/XMIT
                 ; character, transmitter enabled)
OUT     06,A     ; (send the A8H to register 5)
; (set up baud rate generator)
LD      A,07H    ; (07H will set the baud rate generator to 1200 baud)
OUT     00,A     ; (send the 07H to the baud rate generator)
```

For 7 bits/character, even parity, D1 of WR4 must be set to 1.

For 8 bits/character, no parity, set D0 of WR4 to 0. Set D7 and D6 of WR3 both to 1 and set D5 and D6 of WR5 also both to one.

PARALLEL I/O—B3-C3—

The Z80 PIOs are used for a system bitport (SYS PIO) and a Centronics printer port (GP PIO). The system bitport usage was outlined in the introduction of this section.

A Z80 PIO can be programmed to work in 4 different modes.

MODE 1 Output Port
MODE 2 Input Port
MODE 3 Bidirectional Port
MODE 4 Control Port (bitport)

The operation mode is set by sending the chip a byte when the C/D input is high. The lower nibble must be 1111 to instruct the chip that this is a operation mode command. Bits 6 and 7 are decoded by the PIO to determine which mode is to be set.

MODE	D7	D6
0	0	0
1	0	1
2	1	0
3	1	1

A mode 3 command must be followed by another byte which will indicate what direction each bit will be sent. A 1 in a given bit position indicates that the position will be an input bit, while a 0 indicates an output bit. In mode 3 the data strobe is ignored and the ready output is held low.

Interrupt control is also programmable. The low nibble is used to indicate that this is an interrupt command, and it must be 0111. The high nibble indicates the interrupt mode as follows.

BIT	SIGNIFICANCE
D7	ENABLE INTERRUPTS (must be 1 to enable)
D6	AND/OR This selects the logical function to be performed on the unmasked bits in order to allow interrupt enable (1 is AND)
D5	HIGH/LOW This indicates the active polarity of the bits operated on above (1 is HIGH)
D4	MASK FOLLOWS This indicates that the next byte is the interrupt mask
D6-D4	are only used for mode 3 operation

The interrupt enable flag can be set or reset without affecting the other bits in the registers. To do this, the lower nibble is 0011. D7 will then be examined by the PIO to determine how the interrupt flag. A 0 will disable interrupts.

To load an interrupt vector, D0 must be a 0. This informs the PIO that the remaining bits (D1-D7) are an interrupt vector. The PIO then loads the vector into its vector register exactly as it appears.

The KayPro can use the unused PIO ports in any configuration. The system bitport must be used as it is set by the monitor. The Centronics port could be changed, but it is buffered to the connector by unidirectional line drivers.

FLOPPY DISK CONTROLLER—C2-D2—

The KayPro II uses a 1793 floppy disk controller, U83. The 1793 only needs two external chips. It requires a 1 Mhz clock to operate. It uses four signals from the floppy disk drives—Track 0, Write Protect, Index, and the Raw Data from the read head. The controller provides the floppy disk drives with some control signals and the rest are provided by the system bit port. The signals originating from the controller are Write Gate, Step, and Direction. The write data and precompensation information are fed to one of the external chips which provides the properly timed write data.

DATA SEPARATION—D1—

The data stream from the floppy disk is made up of two components, clock and data. The 1793 is not capable of separating these two components, so U88 is used to remove the clock pulses from the data stream. U88 provides the separate data and clock signals to the 1793.

WRITE PRECOMPENSATION—C1—

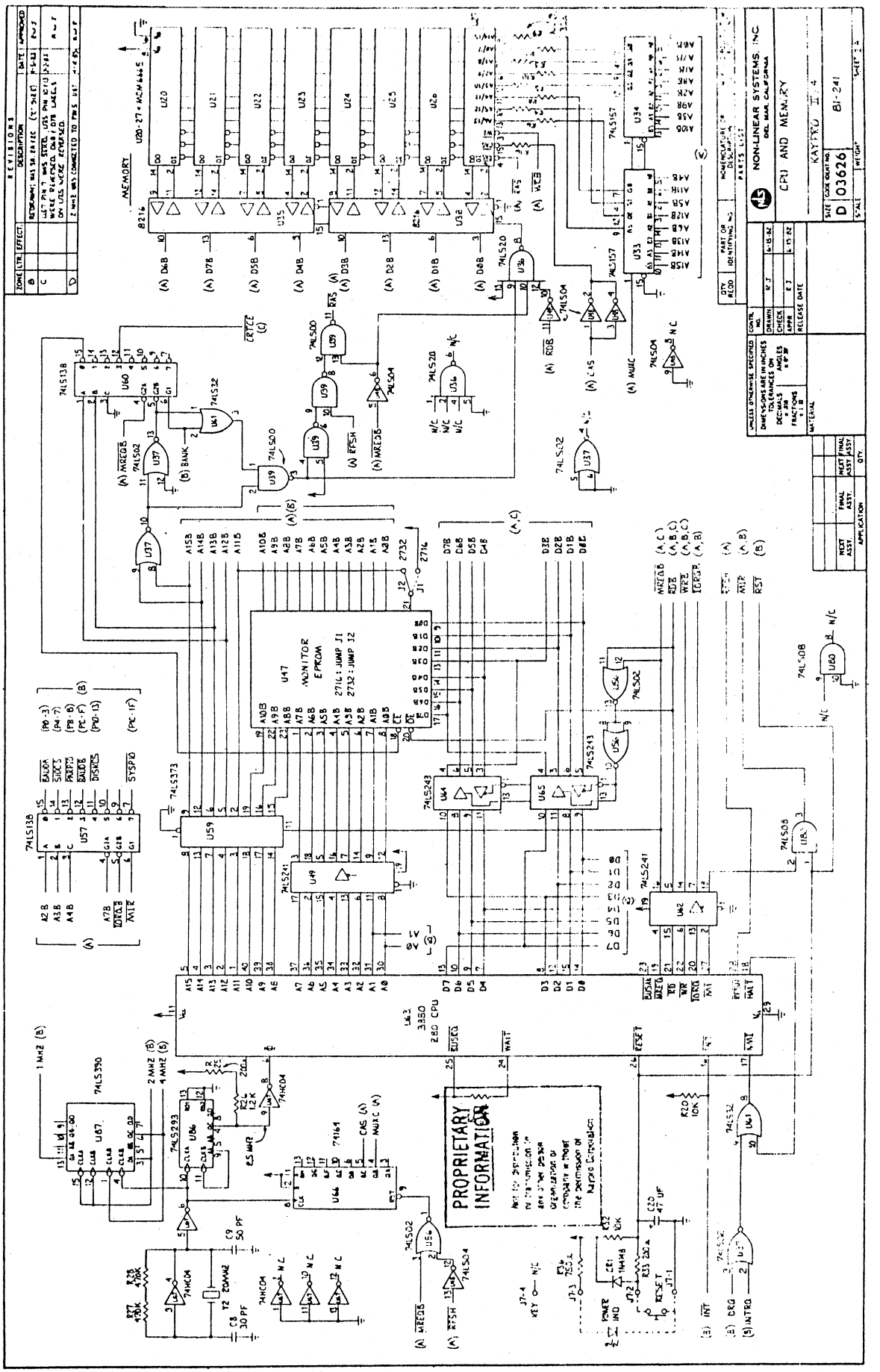
U84, a shift register, is used for write precompensation. It uses early and late signals from the 1793 to determine the direction of shift. If both early and late are low, the shift register is loaded through the B input. An early signal causes the data to be shifted early, which means it will arrive at the write head sooner.

Precompensation makes up for the difference in head to disk speed between the inner and outer tracks. The shift register is loaded by the Write Data output of the 1793 and clocked by the 4 Mhz clock. U85 is used to change the active high Write Data pulse into an active low Load pulse.

U#	Device	Grid Loc.	Description
Y3	CRYSTAL	A2	5.0688 Mhz crystal
U52	74LS241	C2	Octal buffers/line drivers
U54	3881	C3	Z80 programmable parallel I/O
U57	74LS138	A3	3 to 8 line decoders
U62	74LS241	D1	Octal buffers/line drivers
U68	MC1488	B1	High voltage inverting line drivers
U69	MC1489	B1	High voltage inverting line receivers
U70	3884	B2	Z80 programmable serial I/O
U71	74S04	B1	Hex inverters
U72	3881	B3	Z80 programmable parallel I/O
U73	74LS04	C1,C2,A2	Hex inverters
U76		D1	1K x 7 SIP resistors
U78	8116	A2	Programmable baud clock generator
U81	7406	C1,C2	Hex inverters
U82	1793/7	C2-D2	Floppy disk controller
U84	74LS195	C1	4 bit parallel access shift register
U85	74LS02	C1	Quad 2 input positive NOR
U88	9216	D1	External data separator

errata

Though (almost) every attempt was made to verify and double check the schematic, something was missed before the schematic went to print. The inverter (U73) in grid A2 is labled 74LS14. It should have been labled 74LS04.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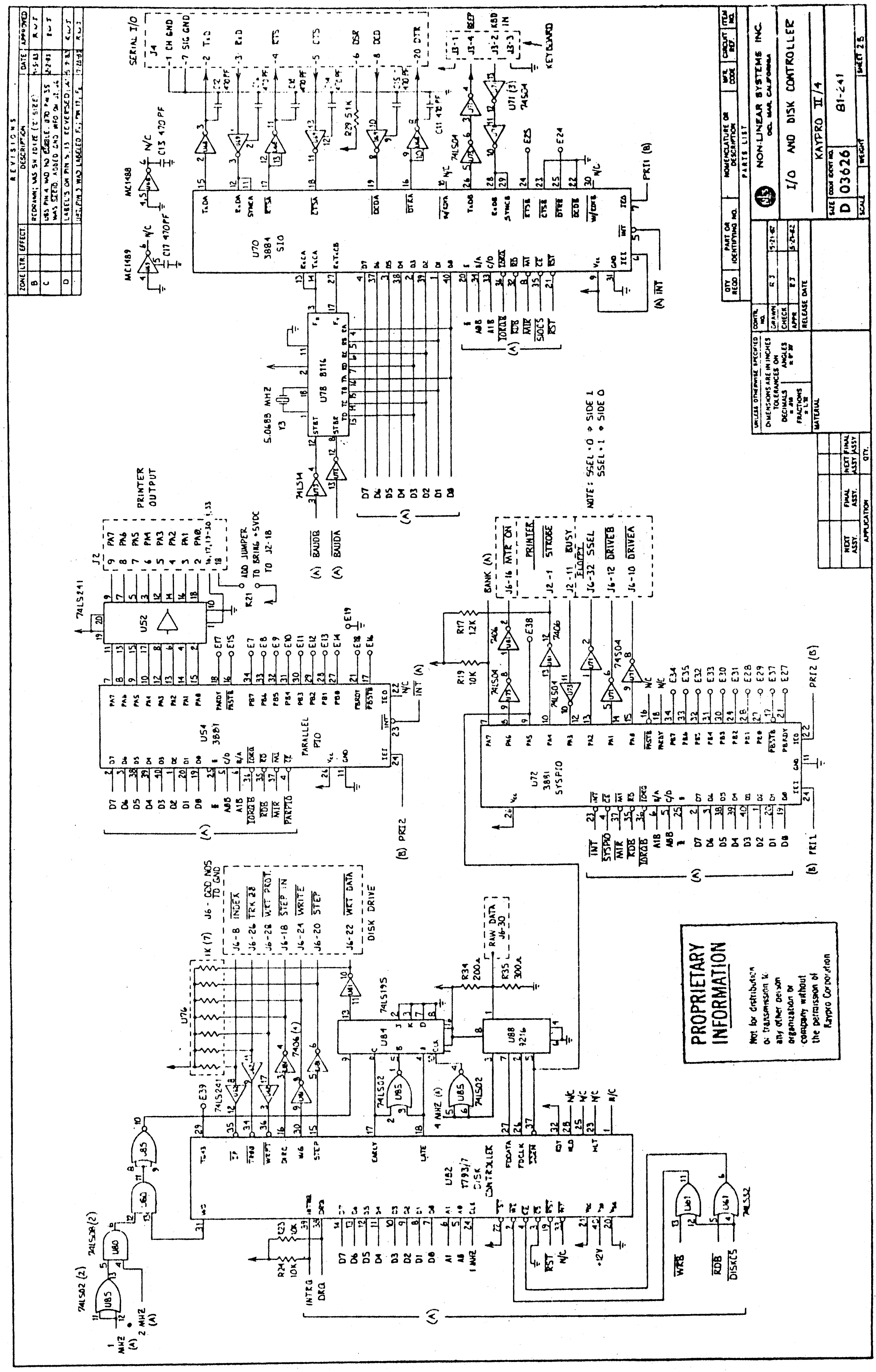
KAYPRO II
D 03626
81-241
PROPRIETARY INFORMATION
MONITOR EPROM
2716 : JUMP J1
2732 : JUMP J2
Z80 CPU
74LS138
74LS373
74LS241
74LS245
74LS32
74LS02
74LS08
74LS04
74LS00
74LS20
74LS157
74LS390
74LS393
74HC04
74164
MEMORY



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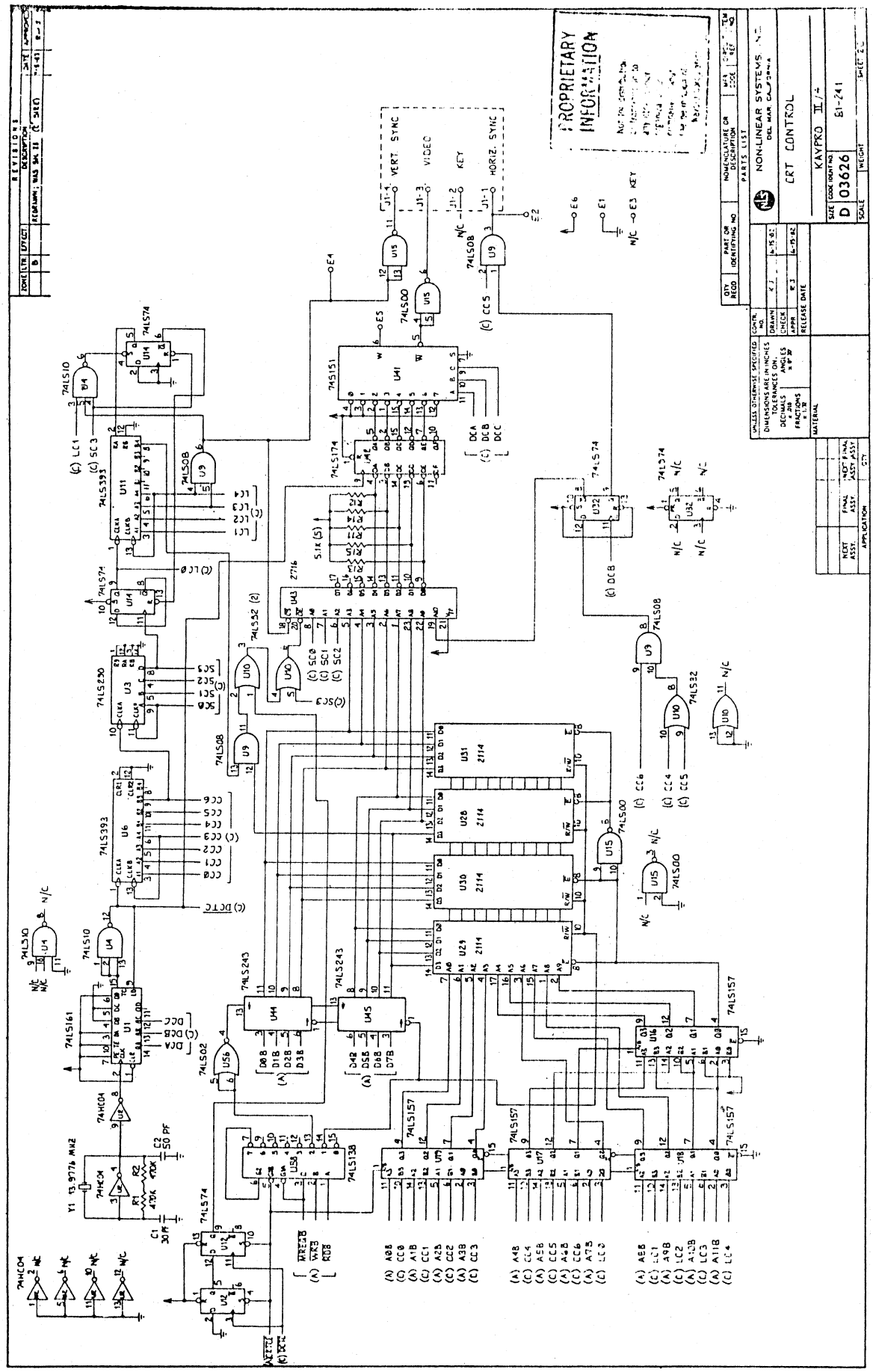
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